SST-50 W LEDs

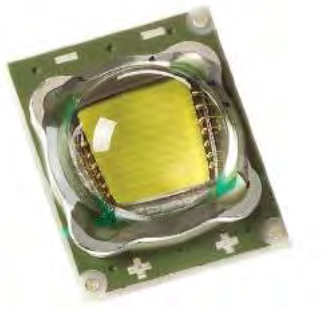

Table of Contents

Features:

- Extremely high optical output: Over 1,150 lumens from a single chip (white)
- Extremely high efficiency: Over 100 lumens per watt at 1.75A
- High thermal conductivity package - junction to case thermal resistance of only 2.45 °C/W
- Large, monolithic chip with uniform emitting area of 5 mm^2
- Lumen maintenance of greater than 70% after 60,000 hours
- Environmentally friendly: RoHS compliant
- Variable drive currents: less than 1 A through 5 A
- High reliability
- Electrically isolated thermal path

Applications

- Replacement Lamps
- High Bay Lighting
- Street Lighting
- Consumer Portable
- Architectural Lighting
- Retail Lighting
- Residential Lighting
- Spot Lighting

PDS-001345Rev 07

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Technology Overview

Luminus Big Chip LEDs™ benefit from a suite of innovations in the fields of chip technology, packaging and thermal management. These breakthroughs allow illumination engineers and designers to achieve solutions that are high brightness and high efficiency.

Photonic Lattice Technology

Luminus' photonic lattice technology enables large area LED chips with uniform brightness over the entire LED chip surface. The optical power and brightness produced by these large monolithic chips enable solutions which replace arc and halogen lamps where arrays of traditional high power LEDs cannot.

For red, green and blue LEDs, the photonic lattice structures extract more light and create radiation patterns that are more collimated than traditional LEDs. Having higher collimation from the source increases optical collection efficiencies and simplifies optical designs.

Packaging Technology

Thermal management is critical in high power LED applications. With a thermal resistance from junction to case of 2.45° C/W. Luminus SST-50 LEDs have the lowest thermal resistance of any LED on the market. This allows the LED to be driven at higher current densities while maintaining a low junction temperature, thereby resulting in brighter solutions and longer lifetimes.

Reliability

Designed from the ground up, Luminus Big Chip LEDs are one of the most reliable light sources in the world today. Big Chip LEDs have passed a rigorous suite of environmental and mechanical stress tests, including mechanical shock, vibration, temperature cycling and humidity, and have been fully qualified for use in extreme high power and high current applications. With very low failure rates and median lifetimes that typically exceed 60,000 hours, Luminus Big Chip LEDs are ready for even the most demanding applications.

Environmental Benefits

Luminus LEDs help reduce power consumption and the amount of hazardous waste entering the environment. All Big Chip LED products manufactured by Luminus are RoHS compliant and free of hazardous materials, including lead and mercury.

Understanding Big Chip LED Test Specifications

Every Luminus LED is fully tested to ensure that it meets the high quality standards expected from Luminus' products.

Testing Temperature

Luminus core board products are typically measured in such a way that the characteristics reported agree with how the devices will actually perform when incorporated into a system. This measurement is accomplished by mounting the devices on a 40°C heat sink and allowing the device to reach thermal equilibrium while fully powered. Only after the device reaches equilibrium are the measurements taken. This method of measurement ensures that Luminus Big Chip LEDs perform in the field just as they are specified.

Luminus surface mount LEDs are typically tested with a 20mSec input pulse and a junction temperature of 25°C. Expected flux values in real world operation can be extrapolated based on the information contained within this product data sheet.

Multiple Operating Points (1.75, 5.0 A)

The tables on the following pages provide typical optical and electrical characteristics. Since the LEDs can be operated over a wide range of drive conditions (currents from less than 1.0 A to 5.0 A, and duty cycle from <1% to 100%), multiple drive conditions are listed.

SST-50 LEDs are production tested at 1.75 A. The values shown at 5.0 Aare for additional reference at other possible drive conditions.

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SST-50 White Binning Structure

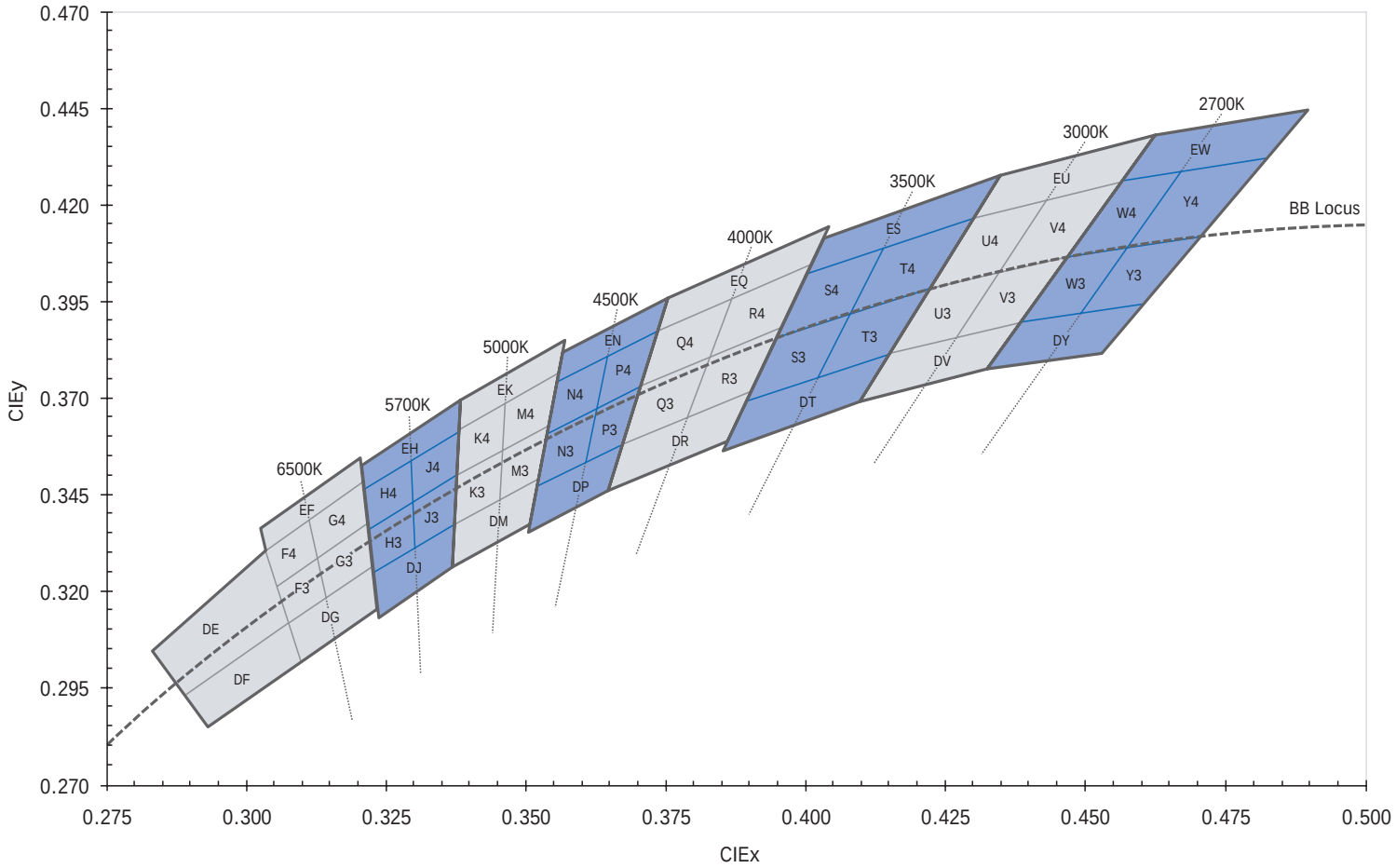
SST-50 LEDs are tested for luminous flux and chromaticity at a drive current of 1.75 A (350 mA/mm^2) and placed into one of the following luminous flux (FF) and chromaticity (WW) bins:

Flux Bin (FF)	Minumum Flux (lm) @ 1.75A	Maximum Flux (lm) @ 1.75A
G2	300	325
G3	325	350
H	350	375
H2	375	400
H3	400	425
J	425	450
J2	450	475
J3	475	500

*Note: Luminus maintains a +/- 6% tolerance on flux measurements.

Chromaticity Bins

Luminus' Standard Chromaticity Bins: 1931 CIE Curve



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The following tables describe the four chromaticity points that bound each chromaticity bin. Chromaticity bins are grouped together based on the color temperature.

6500K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
DG	0.307	0.311
	0.322	0.326
	0.323	0.316
	0.309	0.302
F3*	0.305	0.321
	0.313	0.329
	0.315	0.319
	0.307	0.311
F4*	0.303	0.330
	0.312	0.339
	0.313	0.329
	0.305	0.321
G3*	0.313	0.329
	0.321	0.337
	0.322	0.326
	0.315	0.319
G4*	0.312	0.339
	0.321	0.348
	0.321	0.337
	0.313	0.329
EF	0.302	0.335
	0.320	0.354
	0.321	0.348
	0.303	0.330
DE	0.283	0.304
	0.303	0.330
	0.307	0.311
	0.289	0.293
DF	0.289	0.293
	0.307	0.311
	0.309	0.302
	0.293	0.285

5700K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
DJ	0.322	0.324
	0.337	0.337
	0.336	0.326
	0.323	0.314
H3*	0.321	0.335
	0.329	0.342
	0.329	0.331
	0.322	0.324
H4*	0.321	0.346
	0.329	0.354
	0.329	0.342
	0.321	0.335
J3*	0.329	0.342
	0.337	0.349
	0.337	0.337
	0.330	0.331
J4*	0.329	0.354
	0.338	0.362
	0.337	0.349
	0.329	0.342
EH	0.320	0.352
	0.338	0.368
	0.338	0.362
	0.321	0.346

*Sub-bins within ANSI defined quadrangles per ANSI C78.377-2008

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5000K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
EK	0.338	0.368
	0.356	0.384
	0.355	0.376
	0.338	0.362
K3*	0.337	0.349
	0.345	0.355
	0.345	0.343
	0.337	0.337
K4*	0.338	0.362
	0.347	0.369
	0.345	0.355
	0.337	0.349
M3*	0.345	0.355
	0.353	0.349
	0.352	0.372
	0.344	0.343
M4*	0.346	0.369
	0.355	0.376
	0.353	0.362
	0.345	0.355
DM	0.337	0.337
	0.352	0.349
	0.350	0.337
	0.336	0.326

4500K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
EN	0.356	0.384
	0.376	0.396
	0.374	0.387
	0.355	0.374
N3*	0.353	0.360
	0.361	0.366
	0.359	0.352
	0.351	0.347
N4*	0.355	0.374
	0.364	0.381
	0.361	0.366
	0.353	0.360
P3*	0.361	0.366
	0.370	0.373
	0.367	0.358
	0.359	0.352
P4*	0.364	0.381
	0.374	0.387
	0.370	0.373
	0.361	0.366
DP	0.351	0.347
	0.367	0.358
	0.364	0.346
	0.350	0.335

*Sub-bins within ANSI defined quadrangles per ANSI C78.377-2008

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4000K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
EQ	0.376	0.396
	0.404	0.414
	0.401	0.404
	0.374	0.387
Q3*	0.370	0.373
	0.382	0.380
	0.378	0.365
	0.367	0.358
Q4*	0.374	0.387
	0.387	0.396
	0.382	0.380
	0.370	0.373
R3*	0.382	0.380
	0.395	0.388
	0.390	0.372
	0.378	0.365
R4*	0.387	0.396
	0.401	0.404
	0.395	0.388
	0.382	0.380
DR	0.367	0.358
	0.390	0.372
	0.386	0.359
	0.364	0.346

3500K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
ES	0.403	0.411
	0.435	0.427
	0.430	0.417
	0.400	0.402
S3*	0.394	0.385
	0.407	0.392
	0.402	0.375
	0.389	0.369
S4*	0.400	0.402
	0.415	0.409
	0.407	0.392
	0.394	0.385
T3*	0.407	0.392
	0.422	0.399
	0.415	0.381
	0.402	0.375
T4*	0.415	0.409
	0.430	0.417
	0.422	0.399
	0.407	0.392
DT	0.389	0.369
	0.415	0.381
	0.409	0.369
	0.385	0.357

*Sub-bins within ANSI defined quadrangles per ANSI C78.377-2008

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3000K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
EU	0.435	0.427
	0.462	0.437
	0.456	0.426
	0.430	0.417
U3*	0.422	0.399
	0.434	0.403
	0.426	0.385
	0.415	0.381
U4*	0.430	0.417
	0.443	0.421
	0.434	0.403
	0.422	0.399
V3*	0.434	0.403
	0.447	0.408
	0.437	0.389
	0.426	0.385
V4*	0.443	0.421
	0.456	0.426
	0.447	0.408
	0.434	0.403
DV	0.415	0.381
	0.437	0.389
	0.431	0.377
	0.409	0.369

2700K Chromaticity Bins		
Bin Code (WW)	CIEx	CIEy
EW	0.462	0.437
	0.488	0.444
	0.481	0.432
	0.456	0.426
W3*	0.447	0.408
	0.458	0.410
	0.448	0.392
	0.437	0.389
W4*	0.456	0.426
	0.469	0.429
	0.458	0.410
	0.447	0.408
Y3*	0.458	0.410
	0.70	0.413
	0.459	0.394
	0.448	0.392
Y4*	0.469	0.429
	0.481	0.432
	0.470	0.413
	0.458	0.410
DY	0.437	0.389
	0.459	0.394
	0.452	0.382
	0.431	0.377

*Sub-bins within ANSI defined quadrangles per ANSI C78.377-2008

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Product Shipping & Labeling Information

All SST-50 products are packaged and labeled with their respective bin as outlined in the tables from pages 3 to 7. When shipped, each package will only contain one bin. The part number designation is as follows:

SST — 50 — WNNX — F21 — FF — WW

Product Family	Chip Area	Color	Package Configuration	Flux Bin	Chromaticity Bin
Surface Mount (Lens)	5.0 mm^2	CCT & CRI See Note 1 below	Internal Code	See page 3 for bins	See page 4-7 for bins

Note 1: WNNX nomenclature corresponds to the following:
W = White
NN = color temperature, where:
65 corresponds to 6500K
X = color rendering index, where:
S (standard) corresponds to a typical CRI of 70

Note 2: Some flux and chromaticity bins may have limited availability. Application specific bin kits, consisting of multiple bins, may be available. For ordering information, please refer to page 15 and reference PDS-001848: SST-50 Binning & Labeling document.

Example:
The part number SST-50-W65S-F21-J3-G4 refers to a 6500K standard CRI white, SST-50 emitter, with a flux range from 475 to 500 lumens and a chromaticity value within the box defined by the four points (0.313, 0.338), (0.321, 0.348), (0.322, 0.336), (0.312, 0.328).

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Electrical Characteristics[1]

Optical and Electrical Characteristics (T_J = 25 °C)

Drive Condition[2]		1.75 A	5.0 A	
Parameter	Symbol	Values at Test Currents	Typical Values at Indicated Current[3]	Unit
Current Density	j	0.35	1.0	A/mm^2
Forward Voltage	$V_{F, min}$	2.5		V
	$V_{F, typ}$	3.2	3.6	V
	$V_{F, max}$	3.9		V

Common Characteristics

Parameter	Symbol	Values	Unit
Viewing Angle	$2\theta_{1/2}$	100	
Emitting Area	A	5.0	mm^2
Emitting Area Dimensions		2.25 x 2.25	mm×mm
Forward Voltage Temperature Coefficient[4]		-4.4	mV/°C

Absolute Maximum Ratings

Parameter	Symbol	Values	Unit
Maximum Current[5]		5.0	A
Maximum Reverse Current		N/A	
Maximum Junction Temperature[6]	T_{j-max}	150	°C
Storage Temperature Range		-40/+100	°C

Note 1: Listed drive conditions are typical for common applications. SST-50 White devices can be driven at currents ranging from <1A to 5A and at duty cycles ranging from <1% to 100%. Drive current and duty cycle should be adjusted as necessary to maintain the junction temperature desired to meet application lifetime requirements.

Note 2: Unless otherwise noted, values listed are typical.

Note 3: Forward voltage temperature coefficient at 1.75A. Contact Luminus for value at other drive conditions.

Note 4: SST-50 devices are designed for operation to an absolute maximum forward drive current 5A. Product lifetime data is specified at recommended forward drive currents. Sustained operation at absolute maximum currents will result in a reduction of device lifetime compared to recommended forward drive currents. Actual device lifetimes will also depend on junction temperature. Refer to APN-001521: Reliability Application Note for SST-50-W for further information. In pulsed operation, rise time from 10-90% of forward current should be larger than 0.5 microseconds.

Note 5: Lifetime dependent on LED junction temperature . Thermal calculations based on input power and thermal management system should be performed to ensure T_J is maintained below T_{jmax} rating or life will be reduced. Refer to APN-001521 for further information.

Note 6: CIE measurement uncertainty for white devices is estimated to be +/- 0.01.

Note 7: Special design considerations must be observed for operation under 1A. Please contact Luminus for further information.

Note 8: Caution must be taken not to stare at the light emitted from these LEDs. Under special circumstances, the high intensity could damage the eye.

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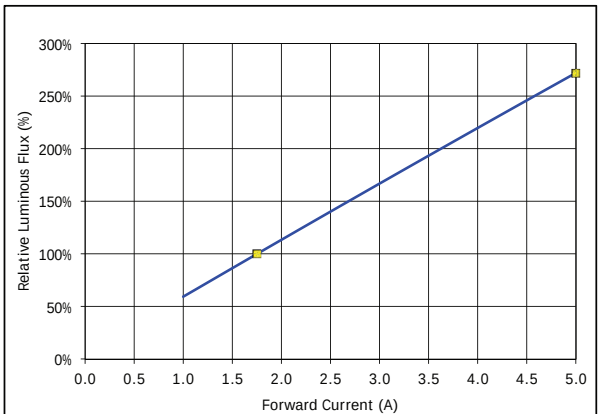
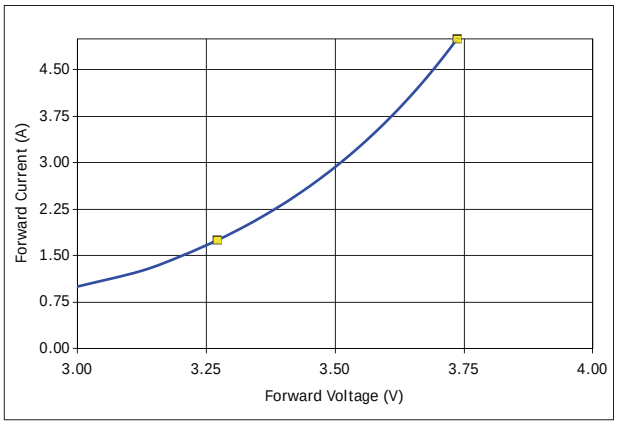
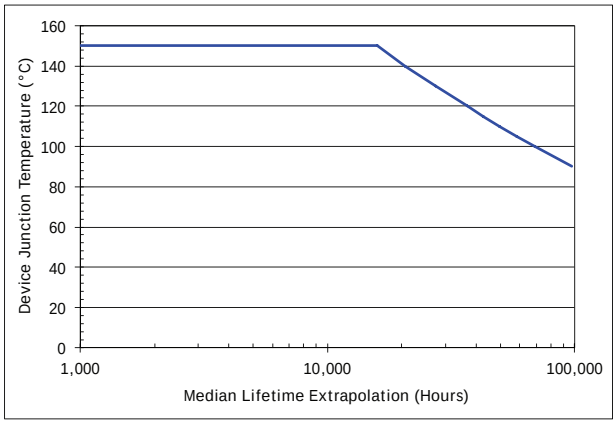
Relative Output Flux vs. Forward Current[1]



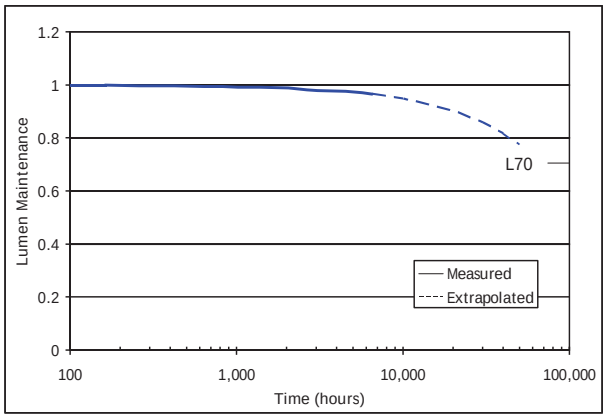
Forward Current vs. Forward Voltage



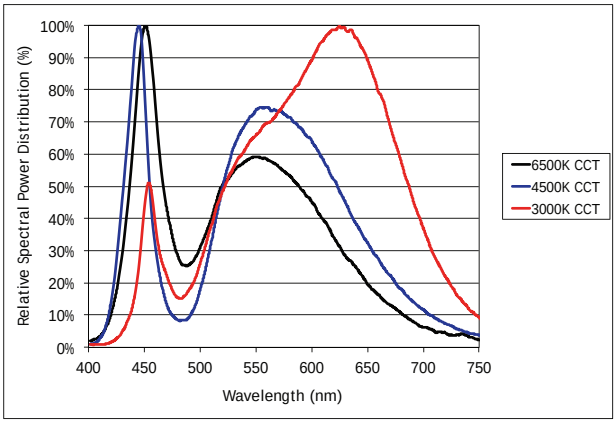
Mean Lifetime[2]



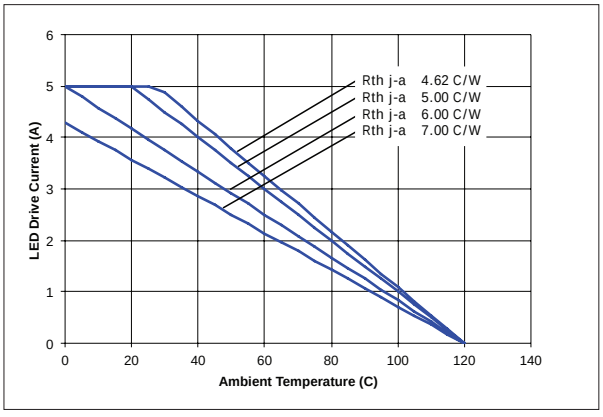
Lumen Maintenance vs. Time[3]



Typical Relative Spectral Power[4]



Current Derating Curve



Note 1: Yellow squares indicate typical operating conditions.

Note 2: Mean expected lifetime in dependence of junction temperature at 0.35 A/mm^2 in continuous operation. Lifetime defined as time to 70% of initial intensity. Based on lifetime test data of uncoated GaN devices at this time. Data can be used to model failure rate over typical product lifetime (contact Luminus for lifetime reliability test data for 1A/mm^2 condition).

Note 3: Lumen maintenance in dependence of time at 0.35 A/mm^2 in continuous operation with junction temperatures of 100 ºC.

Note 4: Typical spectrum at current density of 0.35 A/mm^2 in continuous operation.

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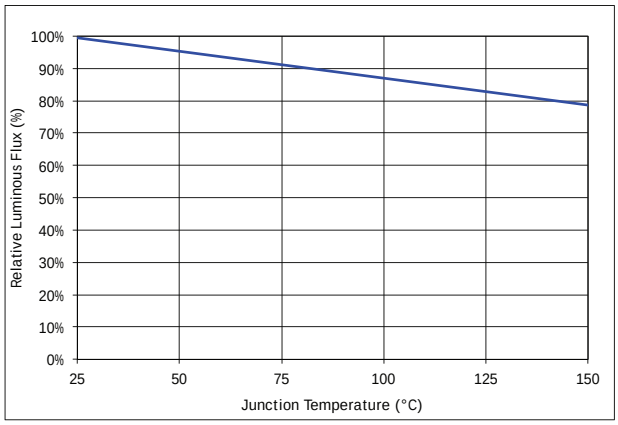
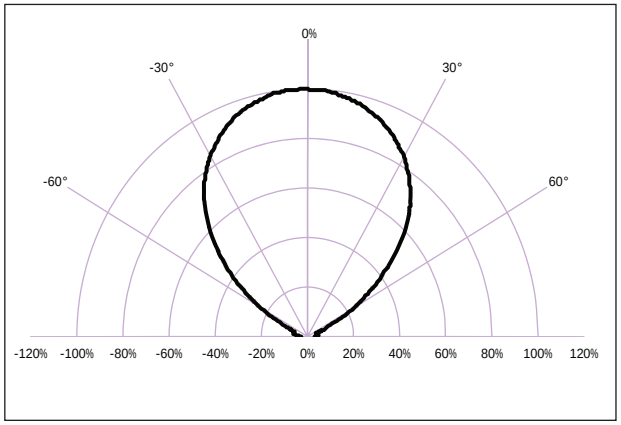
Relative Output Flux vs. Junction Temperature

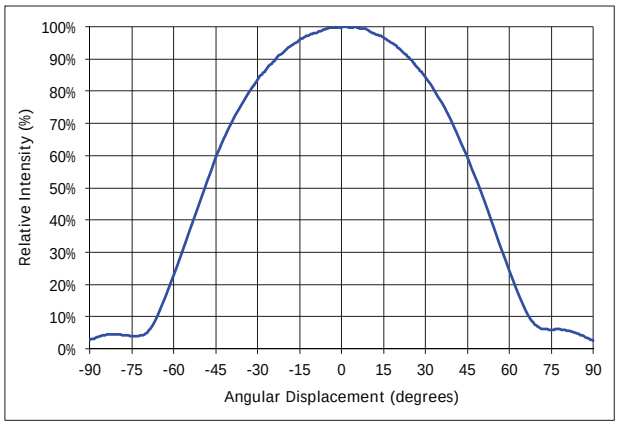


Typical Radiation Pattern

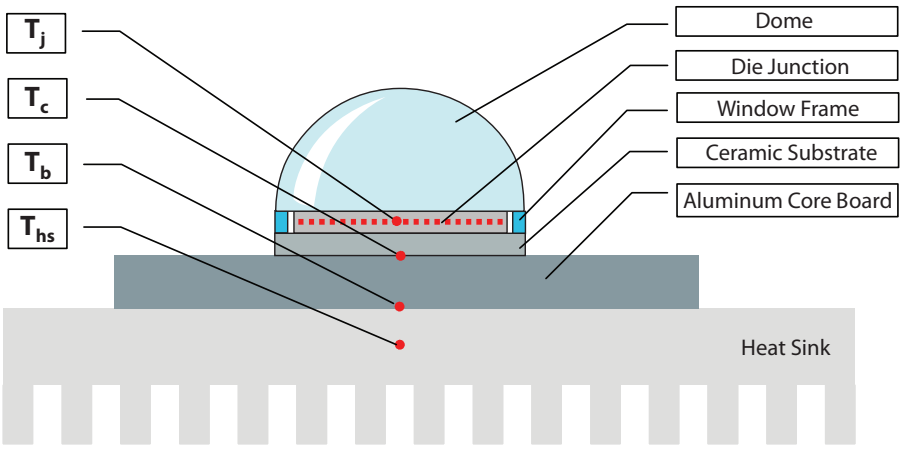
Typical Polar Radiation Pattern for White



Typical Angular Radiation Pattern for White



Thermal Resistance



Typical Thermal Resistance, junction to case

$R_{j\text{-}c}$ [1]	2.45 °C/W
$R_{j\text{-}b}$ [1]	4.28 °C/W
$R_{j\text{-}hs}$ [2]	4.39 °C/W

Note 1: Thermal resistance values are based on FEA model results correlated to measured $R_{\theta j\text{-}hs}$ data.

Note 2: Thermal resistance is measured using a SAC305 solder, a Bergquist Al-clad MCPCB, and eGraf 1205 thermal interface material.

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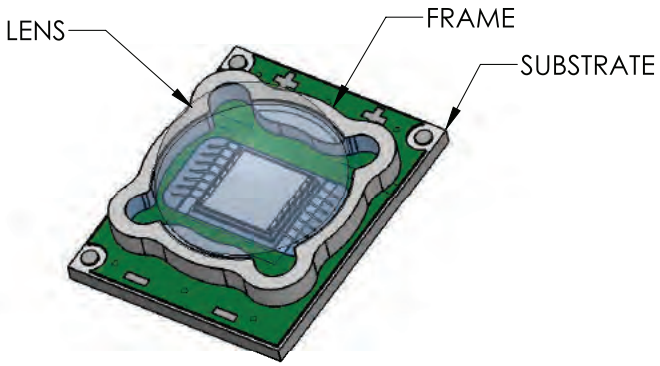
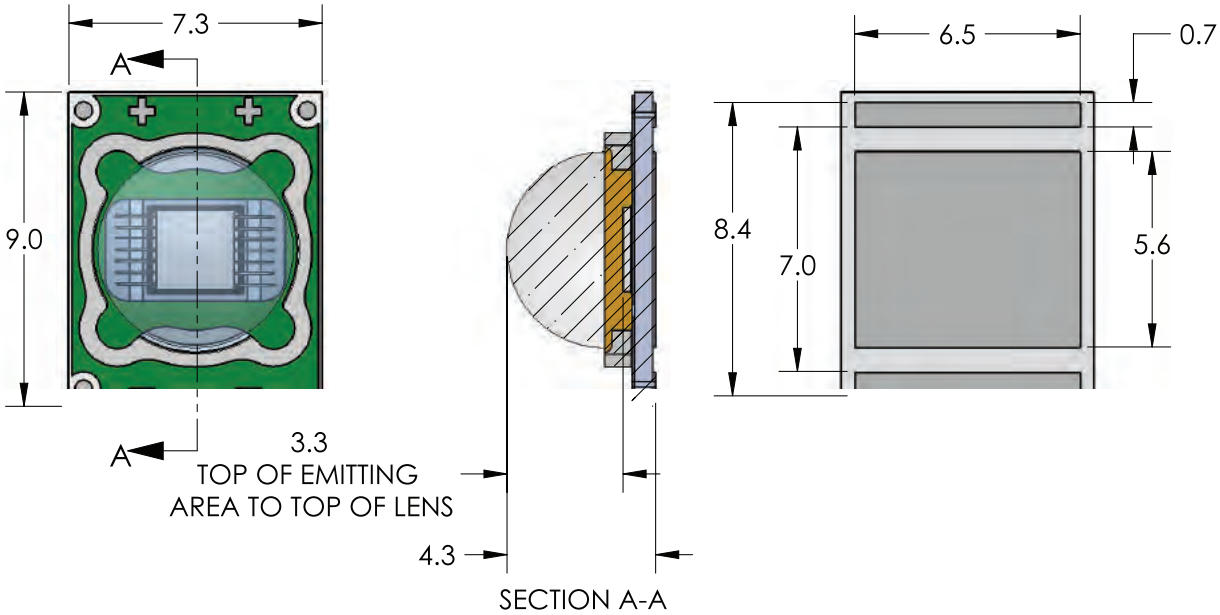
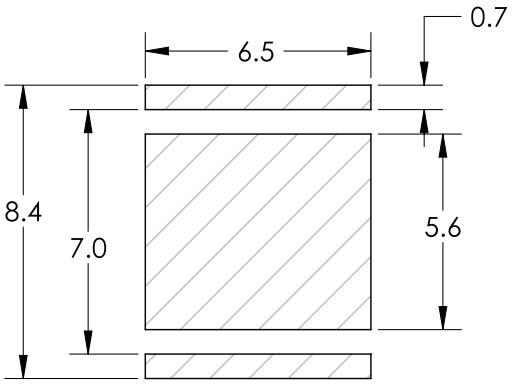
Mechanical Dimensions – SST-50 Emitter

DIMENSIONS IN MILLIMETERS







RECOMMENDED SOLDER PAD

For detailed drawing please refer to DWG-001358 document

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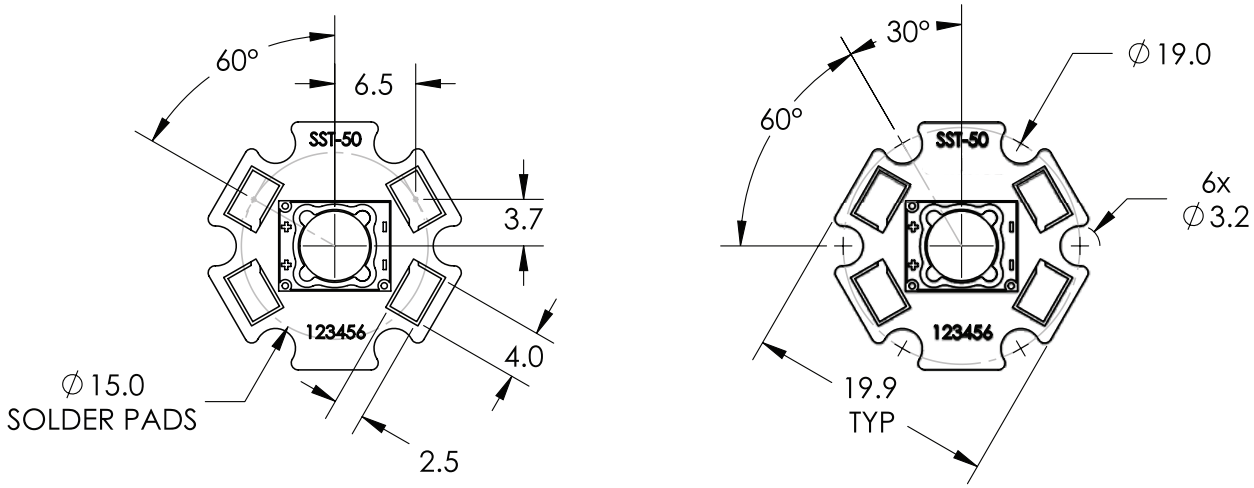
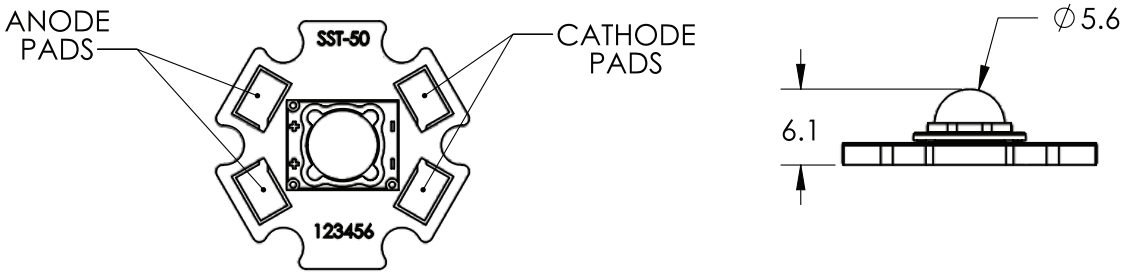
Mechanical Dimensions – SST-50 Star Board





Note 1: Recommended mounting screw: M3 or #4

Note 2: All dimensions in millimeters

Note 3: anode pads on board are interconnected. All cathode pads on board are interconnected

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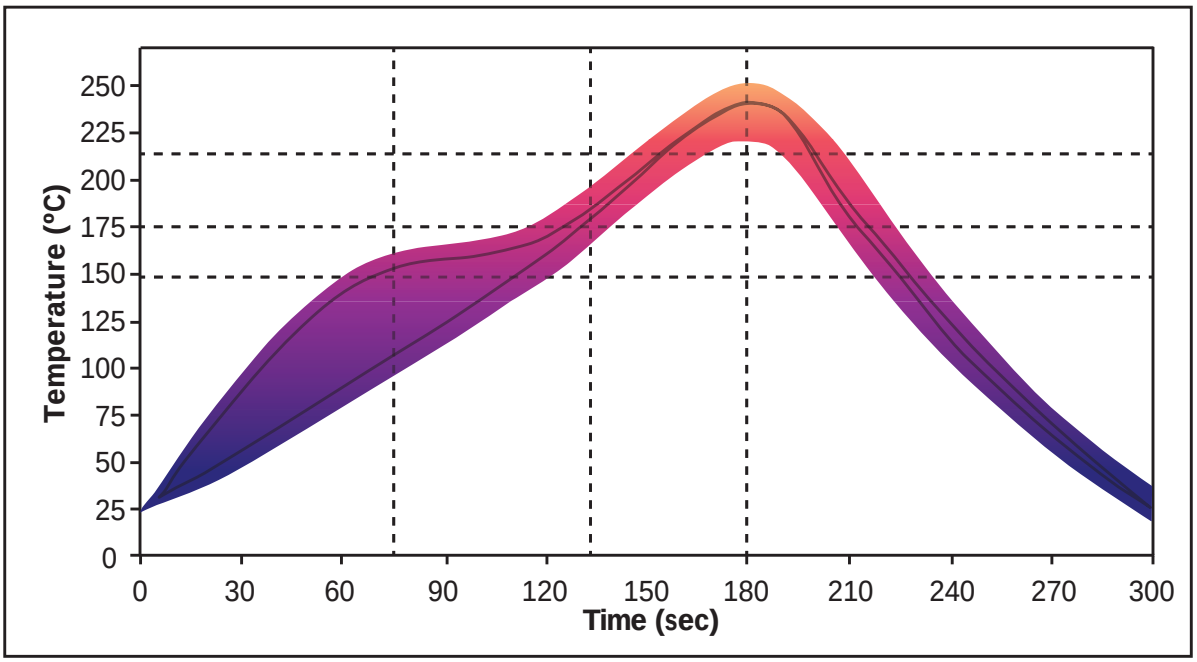
Solder Profile

SAC 305 Reflow Profile Window For Low Density Boards



Lead free solder guideline for low density boards

Solder Profile Stage	Lead-Free Solder	Lead-based Solder
Profile length, Ambient to Peak	2.75 - 3.5 minutes	2.75 - 3.5 minutes
Time Maintained Above: Temperature	217 °C	217 °C
Time Maintained Above: Time	30 - 60 seconds	30 - 60 seconds
Cooldown Rate	≤4° C/sec	≤4° C/sec
Cooldown Duration	45 ± 15 sec	45 ± 15 sec

Note 1: Temperatures are taken and monitored at the component copper layer.

Note 2: Optimum profile may differ due to oven type, circuit board or assembly layout.

Note 3: Recommended lead free, no-clean solder: AIM NC254-SAC305.

Note 4: Refer to APN-001473 soldering and handling application note for additional solder profiles and details.

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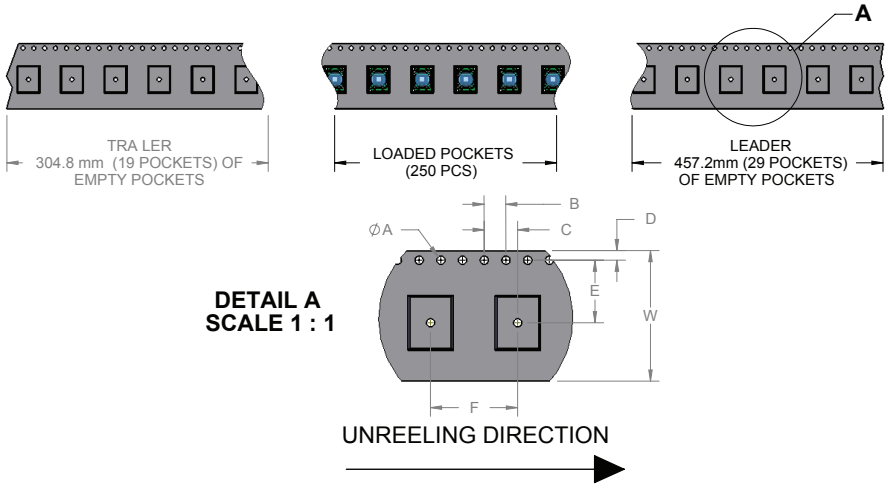
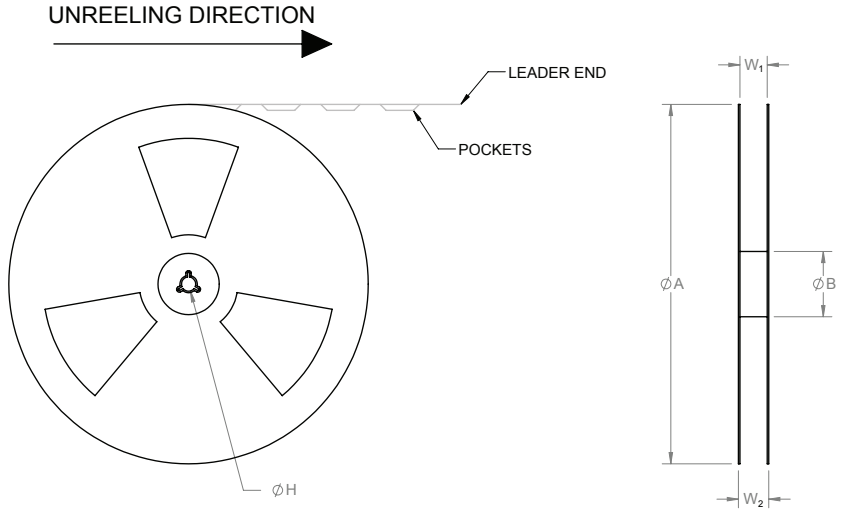
Tape and Reel Drawing of SST-50

DIMENSIONS ARE IN mm. (INCH)



TAPE DIMENSIONS						
W	∅A	B	C	D	E	F
24.0 (.945)	1.5 (.059)	3.9 (.157)	6.1 (.241)	1.7 (.069)	11.5 (.453)	16.0 (.630)



REEL DIMENSIONS				
∅A	W_1	W_2	∅B	∅H
∅330.2 (13.0)	25 (.984)	27.8 (1.094)	60.0 (2.362)	∅13.0 (.512)

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Ordering Information

Ordering Part Number [1,2]	Color	Description
SST-50-WDLS-F21/T21-GG150	6500K White 5700K White	White Big Chip LED™ SST-50 surface mount device consisting of a 5mm^2 LED on a ceramic substrate, F21- tray pack, T21- tape & reel pack
SST-50-WCLS-F21/T21-GG350	5000K White 4500K White	
SST-50-WWTM-F21/T21-GF550	4000K White 3500K White	
SST-50-WWRM-F21/T21-GF750	3000K White 2700K White	
SSR-50-WDLS-R21-GG150	6500K White 5700K White	SSR-50 evaluation module consisting of a SST-50 surface mount device mounted on an aluminum star board
SSR-50-WCLS-R21-GG350	5000K White 4500K White	
SSR-50-WWTM-R21-GF550	4000K White 3500K White	
SSR-50-WWRM-R21-GF750	3000K White 2700K White	

Note 1: GG150 - denotes a bin kit comprising of all flux and chromaticity bins at the 6500K and 5700K color points

GG350 - denotes a bin kit comprising of all flux and chromaticity bins at the 5000K and 4500K color points

GF550 - denotes a bin kit comprising of all flux and chromaticity bins at the 4000K and 3500K color points

GF750 - denotes a bin kit comprising of all flux and chromaticity bins at the 3000K and 2700K color points

Note 2: For ordering information on all available bin kits, please see PDS-001848: SST-50 Binning & Labeling document

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